IN THE CLAIMS:

Please amend the claims to read as follows:

Claim 1 (Currently Amended): A semiconductor device, comprising:

a first interconnect layer disposed over a substrate where a functional semiconductor device is formed;

an inter layer dielectric directly covering a portion of top surface and side surfaces of said first interconnect layer;

a silicon nitride film formed so as to cover entirely a top surface of said inter layer dielectric;

a metal interconnect layer covering said silicon nitride film, said metal interconnect layer being consisted of gold material and serving as a bonding pad; and

a planarized polyimide which is formed directly on a surface of the silicon nitride film, directly surrounding the metal interconnect layer including a surface and a side wall thereof, and serves as a passivation film,

wherein a portion of the planarized polyimide is removed at a part of a region of the surface of the metal interconnect layer, thereby the part of the region of the surface of the metal interconnect layer is exposed from the planarized polyimide, and a bonding wire is connected to the exposed part of the region of the surface of the metal interconnect layer,

wherein a projection area of said region connected with the bonding wire is overlapped with said functional semiconductor device[[; and]] .

~~wherein an organic SOG layer formed by Spin On Glass method lies between the inter layer dielectric and the silicon nitride film~~

wherein the inter layer dielectric includes a first inter layer dielectric formed on the first interconnect layer and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric is thinner than the second inter layer dielectric, and

wherein a sum of a thickness of the first interconnect layer and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric.

Claim 2 (Canceled).

Claim 3 (Previously Presented): A semiconductor device according to claim 1, wherein said silicon nitride film is formed by high-density plasma CVD method.

Claim 4 (Canceled).

Claim 5 (Withdrawn): A method for manufacturing a semiconductor device comprising steps of:

a process for forming a foundation interconnect layer on a surface of a semiconductor substrate on which a functional semiconductor region is formed;

a process for forming an inter layer dielectric on said foundation interconnect layer of which surface is shaped as convex and concave shape;

a process for forming silicon nitride film on said inter layer dielectric;

a process for forming metal interconnect layer as an uppermost layer interconnectas an upper layer of said silicon nitride film, said metal interconnect layer being consisted of gold; and

a process for coating a polyimide resin film on said metal interconnect layer and planarizing surface thereof.

Claim 6 (Withdrawn): A method for manufacturing a semiconductor device according to claim 5, wherein said metal interconnect layer is connected to said foundation interconnect layer through a though hole formed in-between thereof and further wherein said interconnect layer is low in resistance and formed thicker than thickness of said foundation interconnect layer.

Claim 7 (Withdrawn): A method for manufacturing a semiconductor device according to claim 6, wherein said method further includes a process for removing a part of region of said polyimide resin layer, and a process for wire-bonding at said part of region so as to connect to a surface of said metal interconnect layer.

Claim 8 (Currently Amended): A semiconductor device, comprising:

a first interconnect layer covering a first portion of a surface of a functional semiconductor device;

an inter layer dielectric covering a second portion of the surface of the functional semiconductor region and directly covering a portion of top surface and side surfaces of said first interconnect layer, thereby defining a contacting hole on the surface of the first interconnect layer;

a silicon nitride film covering an entire top surface of said inter layer dielectric around the contacting hole on the surface of the first interconnect layer;

a barrier layer covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region;

a metal interconnect layer consisting of gold material covering the barrier layer region, thereby forming a metal interconnect region and serving as a bonding pad; and

a planarized polyimide which is formed directly on a surface of the silicon nitride film, directly surrounding the metal interconnect layer including a surface and a side wall thereof, and serving as a passivation film,

wherein a portion of the planarized polyimide is removed at a part of a region <u>of</u> the surface of the metal interconnect layer, thereby the part of the region of the surface of the metal interconnect layer is exposed from the planarized polyimide, and a bonding wire is connected to the exposed part of the region of the surface of the metal interconnect layer,

wherein a projection area of said region connected with the bonding wire is overlapped with said functional semiconductor device[[; and]] <u>.</u>

~~wherein an organic SOG layer formed by Spin On Glass method lies between the inter layer dielectric and the silicon nitride film~~

wherein the inter layer dielectric includes a first inter layer dielectric formed on the first interconnect layer and a second inter layer dielectric formed on a periphery of the first interconnect layer, and the first inter layer dielectric is thinner than the second inter layer dielectric, and

wherein a sum of a thickness of the first interconnect layer and a thickness of the first inter layer dielectric is substantially same as a thickness of the second inter layer dielectric.

Claim 9 (Previously Presented): The semiconductor device of claim 8, wherein the barrier layer consists of titanium.

Claim 10 (Previously Presented): The semiconductor device of claim 9, wherein the first interconnect layer consists of aluminum.

Claim 11 (Previously Presented): The semiconductor device of claim 8, wherein the first interconnect layer consists of aluminum.

Claim 12 (Previously Presented): The semiconductor device of claim 8, wherein the inter layer dielectric consists of USG film.

Claim 13 (Previously Presented): The semiconductor device of claim 8, wherein the functional semiconductor region further comprises a polysilicon gate isolated from the first

interconnect layer by a third dielectric layer, wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the third dielectric layer.

Claim 14 (Previously Presented): The semiconductor device of claim 1, wherein the planarized polyimide is removed only at the part of the region of the surface of the metal interconnect layer, thereby the metal interconnect layer includes a part of the surface exposed from the planarized polyimide and a part of the surface coated with the planarized polyimide.

Claim 15 (Previously Presented): The semiconductor device of claim 8, wherein the planarized polyimide is removed only at the part of the region of the surface of the metal interconnect layer, thereby the metal interconnect layer includes a part of the surface exposed from the planarized polyimide and a part of the surface coated with the planarized polyimide.